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Latest Trends in Parts SEP Susceptibility from Heavy Ions

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JPL and Aerospace have collected a third set of heavy ion single event phenomena (SEP) test data since their last joint IEEE publications in December 1985 and December 1987. Trends in SEP susceptibility (e.g., soft errors and latchup) for state-of-the-art parts are presented.

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PREFACE

The authors at Jet Propulsion Laboratory thank Jim Coss, single-event upset group leader; William Price, Mark Huebner, Carl Malone, Harvey Schwartz, Kevin Watson, Peter Wang, Mike Havener, and Mike O'Connor.

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I. INTRODUCTION

An ongoing single-event phenomena (SEP) test program at the Jet Propulsion Laboratory (JPL) and The Aerospace Corporation is continuing, in order to assess specific parts performance for interplanetary and satellite environments and to establish trends in single-event upset (SEU) response of an ever-increasing body of device data.

In 1985, Nichols et al.[1] published the first nearly comprehensive listing of SEP test data for 186 parts. This presentation was updated in 1987[2] with the publication of data for 83 additional parts. In this report, we extend the data base for 154 new parts. As before, the data are collected according to technology, function, and manufacturer in order to permit trends, generalizations, and data gaps to be identified.

II. TESTING APPROACHES

The experimental procedures used by JPL and Aerospace are evolutionary and are described in detail elsewhere.[3,4] All data reported here use high energy accelerators—not isotope or other simulation sources. A heavy ion beam of suitable uniformity is directed into a vacuum chamber, where a movable test board and testing interface are mounted. Dosimetry is usually provided by the test group, but the Battelle Northwest Laboratories (BNL) facility now offers this service for their dedicated SEP line. Test interfaces are unique to each part, although some attempts have been made to design "universal interfaces." Tests of complex parts, such as large-scale integration (LSI) random access memories (RAMs) and microprocessors, require special care and usually do not entail a test of every element for every code configuration. Microprocessor tests, for example, might be chosen to yield worst-case linear energy transfer (LET) data (equivalent to the LET threshold for the whole device) and not to yield the overall device cross section.

Tests for transient effects—defined as those disturbances that last for a finite time—are occasionally implemented at the same time as tests for their "infinite" lived cousins—the SEU. Transient effects are not often reported, probably because test procedures are often not set up to measure them—not because of a general scarcity of this phenomenon. Transients are also more elusive than SEUs: they depend upon on-chip design, layout geometries, and other configuration aspects that may mask or augment their detection.

Both transients and "soft" upsets should be of concern to the system designer. Catastrophic effects like latchup, transistor burnout, and other permanent effects require a separate system evaluation.

III. ORGANIZATION AND SCOPE OF DATA

This report summarizes soft error and latchup experimental test data from JPL and The Aerospace Corporation during the 2-year period from January 1987 through December 1988. In addition, data from the Combined Release and Radiation Effects Satellite (CRRES) program, stored at JPL for the last several years, is released for the first time—except for proprietary developmental data on GaAs devices. Not included are data generated by Defense Nuclear Agency (DNA) subcontractors who used JPL hardware, nor the new, fairly extensive data set on power metal-oxide semiconductor field-effect transistor (MOSFET) burnout obtained by other subcontractors. Much smaller SEP data sets have been generated by other U.S. and foreign researchers.[5] The SEP data presented here and in two previous reports[1,2] represent a substantial majority of all test data obtained on SEP throughout the world.

The data from JPL and Aerospace are combined in this report, but there are minor differences in the data from each organization. JPL defines the threshold LET as that value of LET where soft errors are first counted at fluences of 10^6 ions/cm^2. Aerospace has redefined their LET threshold as occurring at that point where the measured upset cross section is 1% of the measured maximum cross section. These two values may be quite different.* To obtain accurate SEU rates for a prescribed radiation environment, one requires a plot of cross section vs LET, which may be available from the parent test organization.**

The data are conveniently divided into two tables: Table 1 for metal-oxide semiconductor (MOS) devices and Table 2 for bipolar devices. All data listed are substantially abbreviated and ignore statistical features altogether. SEP tests are measured with a dynamic nominal bias; latchup tests are performed at the maximum value of the nominal bias range in order to enhance the possibility of latchup. Cross sections are given for Kr ions at normal incidence, corresponding to LET = 37 MeV/mg/cm^2. The label "no upset" also refers to the situation at LET = 37. For devices having a low LET threshold, the tabulated cross section may be equal to the maximum saturation cross section; but at higher LETs, the maximum cross section will be larger than the tabulated value (and may or may not have been found). Unreported transients and higher test temperature measurements exist for some parts. Hence, a system designer interested in a specific part is again urged to contact the appropriate test organization for further information.

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* The use of a LET threshold defined as a stated percentage of a maximum (saturated) cross section attempts to establish a practical lower bound for the purpose of estimating upset rates. The discrepancy between this definition and JPL's definition becomes academic when a complete cross section is used in rate calculations.

** At JPL, more detailed data are available in Reference 6 or in the RADATA computer bank.

Table 1. SEU Data (MOS & CMOS Devices) - 1987 & 1988

Test Org*	Device	Function	Technology	Mfr.	Bits	Effective LET** Threshold (MeV/mg/cm^2)	Device Cross Section (cm^2) ***	Cross Section Per Bit (10^{-8} cm^2)	Facility ****	Remarks (Test Date)
A	Z84C00	Micro P (8-Bit)	CMOS	Z1L	--	--	--	--	88-in.	Latchup at LET = 25; cross section = 2.5 x 10^{-3} cm^2 (June, 1988)
J	SA3300	16-Bit Micro P	CMOS/bulk No resistor	SNL	--	≤0 ±6	--	--	BNL	Clone of NS32016 (Aug, Oct, 1988) High Temp Data Available
J	SA3300	16-Bit Micro P	CMOS/bulk With resistor	SNL	--	>120	No upset	--	BNL	Clone of NS32016 (Oct, 1988) High Temp Data Available
J	SA3304	Timing Control Unit (Peripheral)	CMOS/bulk Twin Well	SNL	--	<60	--	--	BNL	Like NS32201 (Oct, 1988)
J	SA3294	Octal D-Latch	CMOS/bulk Twin Well	SNL	--	>120	No upset	--	BNL	Like 54LS373 (Oct, 1988)
J	SA3295	3 by 8 Decoder	CMOS/bulk Twin Well	SNL	--	>120	No upset	--	BNL	Like 54LS138 (Oct, 1988)
J	SA3297	Octal Bus Transceiver	CMOS/bulk Twin Well	SNL	--	>120	No upset	--	BNL	Like 54LS245 (Oct, 1988)
A	HS80C85RH/ SA3000	8-bit Micro P	CMOS/epi	SNL/HAR	93	35[5Vbias] 60[10Vbias]	10^{-4} No upset	--	88-in.	Two parts are identical (Mar, 1987)
J	HS80C85RH SA3000	8-bit Micro P	CMOS/epi	SNL/HAR	93	50[5Vbias] >75[10Vbias]	No upset No upset	--	BNL	Two parts are identical (Jun, 1987)
J/A & ESA	80C86	16-bit Micro P	CMOS/epi	HAR	~600	≤3	6 x 10^{-2}	10,000	88-in. ESA	Developmental Parts. See Nichols et al, IEEE NS (Dec 1988) (Aug, Oct, 1987 & Dec 1988)
J	HS82C37ARH	DMA Controller (80C86 Peripheral)	CMOS Junction Isolation	HAR	~597	9	5 x 15^{-4} (extrap.)	--	BNL	Dynamic Test Mode 344 bits tested (May & Dec, 1988)
ESA	T414	32-bit Micro P	CMOS/bulk	INM	16K(RAM)	3	0.2	200 (RAM)	--	Latchup (1988)
ESA	T414	32-bit Micro P	CMOS/epi	INM	16K(RAM)	3	0.2	200 (RAM)	--	No latchup (1988)
J	80386	32-bit Micro P	CMOS/epi [CHMOS III]	INT	~4000 (tested)	--	--	--	88-in.	No latchup at LET = 40 (July, 1988)
IBM	80386	32-bit Micro P	CMOS/epi [CHMOS III]	INT	~3627	8.5	--	100	BNL	No latchup, LET = 62
IBM	80386	32-bit Micro P	CMOS/epi [CHMOS IV]	INT	~3627	7	--	100	BNL	Latchup
JH	80186	16-bit Micro P	NMOS	INT	~10,000	0.4	5 x 10^{-4}	--	BNL	(1988)
A	8085AH	8-bit Micro P	NMOS	INT	--	<3	>3 x 10^{-3}	--	88-in.	(1987)

*J = JPL, A = Aerospace, LSI = LSI Logic Corp., JH = John Hopkins University, ESA = European Space Agency, and IBM = IBM (Manassas, Va).

**LET = Linear Energy Transfer. Cosine law applied.

***Cross Section (Upsets/Fluence) are given for 120-360 MeV Kr at normal incidence, having an LET = 37 MeV/mg/cm^2. No upset also refers to LET = 37.

****BNL = Brookhaven National Laboratory, Van de Graaff, 88-in. = U.C. Berkeley cyclotron, Orsay = Institut de Physique Nucleaire (cyclotron now defunct).

Table 1. SEU Data (MOS & CMOS Devices) 1987 & 1988 (Continued)

Test Org*	Device	Function	Technology	Mfr.	Bits	Effective LET** Threshold (MeV/mg/cm^2)	Device Cross Section (cm^2) ***	Cross Section Per Bit (10^{-8} cm^2)	Facility ****	Remarks (Test Date)
J	54HC00	Logic	HCMOS	TDX	--	--	--	--	BNL	(5)
J	54HC02	Logic	HCMOS	TDX	--	--	--	--	BNL	(5)
J	54HC04	Logic	HCMOS	TDX	--	--	--	--	BNL	(5)
J	54HC08	Logic	HCMOS	TDX	--	--	--	--	BNL	(5)
J	54HC11	Logic	HCMOS	TDX	--	--	--	--	BNL	(5)
J	54HC20	Logic	HCMOS	TDX	--	--	--	--	BNL	(5)
J	54HC32	Logic	HCMOS	TDX	--	--	--	--	BNL	(5)
J	54HC74	Logic	HCMOS	TDX	--	--	--	--	BNL	(5)
J	54HC85	Logic	HCMOS	TDX	--	--	--	--	BNL	(5)
J	54HC86	Logic	HCMOS	TDX	--	--	--	--	BNL	(5)
J	54HC109	Logic	HCMOS	TDX	--	--	--	--	BNL	(6)
J	54HC125	Logic	HCMOS	TDX	--	--	--	--	BNL	(5)
J/A	54HC138	Logic	HCMOS	TDX	--	.	--	--	BNL	(5); (A = June, 1988)
J	54HC151	Logic	HCMOS	TDX	--	--	--	--	BNL	(6)
J	54HC157	Logic	HCMOS	TDX	--	--	--	--	BNL	(6)
J	54HC161	Logic	HCMOS	TDX	--	--	--	--	BNL	(5) Later vintage than earlier test data.
J	54HC164	Logic	HCMOS	TDX	--	--	--	--	BNL	(5)
J	54HC165	Logic	HCMOS	TDX	--	--	--	--	BNL	(5) Later vintage than earlier test data.
J	54HC193	Logic	HCMOS	TDX	--	--	--	--	BNL	(4)
J/A	54HC244	Logic	HCMOS	TDX	--	--	--	--	BNL	(4) & (6) (A = June, 1988)
J	54HC245	Logic	HCMOS	TDX	--	--	--	--	BNL	(6)
J	54HC280	Logic	HCMOS	TDX	--	--	--	--	BNL	(6)
J	54HC373	Logic	HCMOS	TDX	--	--	--	--	BNL	(5)
J	54HC374	Logic	HCMOS	TDX	--	--	--	--	BNL	(6)
J	54HC00	Logic	HCMOS	STM	--	--	--	--	BNL	(4)
J	54HC138	Logic	HCMOS	STM	--	--	--	--	BNL	(4)
J	54HC174	Logic	HCMOS	STM	--	--	--	--	BNL	(4)
J	54HC373	Logic	HCMOS	STM	--	--	--	--	BNL	(4)
J	54HC390	Logic	HCMOS	STM	--	--	--	--	BNL	(4)
A	CD54HC02	Logic	HCMOS	RCA	--	--	--	--	88-in.	(1)
A	CD54HC73	Logic	HCMOS	RCA	--	--	--	--	88-in.	No latchup at LET = 60 (June, 1988)
A	CD54HC154	Logic	HCMOS	RCA	--	--	--	--	88-in.	(1)
A	CD54HC165	Logic	HCMOS	RCA	8	--	--	--	88-in.	(1)
A	CD54HC299	Logic	HCMOS	RCA	8	--	--	--	88-in.	(1)
A	CD54HC373	Logic	HCMOS	RCA	8	--	--	--	88-in.	(1)
A	MM54HC04	Logic	HCMOS	NSC	--	--	--	--	88-in.	(1)
A	MM54HC151	Logic	HCMOS	NSC	--	--	--	--	88-in.	(1)
A	MM54HC266	Logic	HCMOS	NSC	--	--	--	--	88-in.	(1)

Table 1. SEU Data (MOS & CMOS Devices) 1987 & 1988 (Continued)

Test Org*	Device	Function	Technology	Mfr.	Bits	Effective LET** Threshold (MeV/mg/cm^2)	Device Cross Section (cm^2) ***	Cross Section Per Bit (10^{-8} cm^2)	Facility ****	Remarks (Test Date)
J	54HCT373F	Latch	HCMOS	RCA	8	>75	No Upset	No Upset	BNL	(Dec, 1986)
A	54HCT373	Latch	HCMOS	NSC	8	~80	No Upset	No Upset	SS-in.	No latchup at LET = 120 (Dec, 1988)
A	54HCT541	Octal Buffer	HCMOS	RCA	--	--	--	--	SS-in.	(1)
J	54HCT373C	Latch	HCMOS	STX	8	>75	No Upset	No Upset	Orsay	(Jun, 1985)
J	54HCT244	Tri-State Buffer	HCMOS	TDX	10	--	--	--	SS-in.	No latchup at T = 100°C for LET >168 (Apr, May, 1987)
A	54HCTS161	Counter	HCMOS/SOS	RCA	--	>80	No Upset	No Upset	SS-in.	No latchup at LET = 80 (June, 1988)
A	54HCTS374	D F/F	HCMOS/SOS	RCA	8	>80	No Upset	No Upset	SS-in.	No latchup at LET = 80 (June, 1988)
J	54AC373	Latch	Adv CMOS	FSC	8	--	--	--	SS-in.	Latchup at LET~40 (Aug, 1987)
J	54ACT373	Latch	Adv CMOS	FSC	8	--	--	--	SS-in.	Latchup at LET= 40 (Aug, 1987)
A	54AC138	Logic	Adv CMOS on epi	NSC	--	--	--	--	SS-in.	(3)
A	54AC138	Logic	Adv CMOS	NSC	--	--	--	--	SS-in.	Latchup at ~40; cross section = 10^{-7} cm^2 (Dec, 1988)
A	54AC245	Logic	Adv CMOS on epi	NSC	--	--	--	--	SS-in.	(3)
A	54AC245	Logic	Adv. CMOS	NSC	--	--	--	--	SS-in.	(3)
A	54AC374	Logic	Adv CMOS on epi	NSC	--	~50	No upset	No upset	SS-in.	No latchup at LET = 80 (Dec, 1988)
A	H1546	MUX	CMOS	HAR	--	--	--	--	SS-in.	(1)
A	H1548	MUX	CMOS	HAR	--	--	--	--	SS-in.	(1)
A	H1549	MUX	CMOS	HAR	--	--	--	--	SS-in.	(1)
J	DG507	Quad Analog Switch	CMOS/epi	SIL	4	--	--	--	BNL	No latchup at LET = 120 @ T = 75°C (Dec, 1987)
J	DG125AP	Analog Switch	CMOS/epi	SIL	--	--	--	--	BNL	No latchup at LET = 120 @ T = 125°C (June, 1987)
J	DG125BP	Analog Switch	CMOS/epi	SIL	--	--	--	--	BNL	No latchup at LET = 120 @ T = 125°C (June, 1987)
J	PG303	Analog Switch	CMOS/epi	SIL	--	--	--	--	BNL	No latchup at LET = 120 @ T = 125°C (June, 1987)
J	CD4066B	Quad Bilateral Switch	CMOS	RCA	4	--	--	--	SS-in.	No latchup at LET = 120 @ T = 80°C (Dec, 1987)
A	CS7401	FIFO	CMOS	MMI	256	--	--	--	SS-in.	No latchup at LET = 60 (June, 1988)
A	CY7C401	FIFO	CMOS	CYP	256	--	--	--	SS-in.	Latchup at LET = 10; cross section= 6 x 10^{-4} cm^2 (June, 1988)
A	SSL7401	FIFO	CMOS?	SXT	256	--	--	--	SS-in.	No latchup at LET = 60 (June, 1988)

Table 1. SEU Data (MOS & CMOS Devices) 1987 & 1988 (Continued)

Test Org*	Device	Function	Technology	Mfr.	Bits	Effective LET** Threshold (MeV/mg/cm^2)	Device Cross Section (cm^2) ***	Cross Section Per Bit (10^{-8} cm^2)	Facility ****	Remarks (Test Date)
J	CMM6167	SRAM	CMOS/SOS	RCA	16Kx1	15	4.6×10^{-4}	3	88-in.	$\sigma = 1.4 \times 10^{-3}$ cm^2 for Kr at 20 deg angle. High T data available (Oct, 1987 & June, 1988)
A	IDT6167X	SRAM	NMOS/CMOS	IDT	16Kx1	5	2.6×10^{-2}	165	88-in.	Rad Hard Device. No latchup @ LET = 120 (June 1987)
J	IDT6116V	SRAM	CMOS	IDT	2Kx8	3	10^{-2}	60	BNL	Series A development part Latchup LET = 100 (Feb, 1987)
J/A	IDT6116V	SRAM	NMOS/CMOS	IDT	2Kx8	6	2.5×10^{-2}	160	88-in.	No latchup at LET = 120 (A June 1987, J Aug & Oct, 1987)
A	IDT7187	SRAM	NMOS/CMOS	IDT	64Kx1	5	--	--	88-in.	Rad Hard Device. No latchup at LET = 120 (June, 1987)
A	IDT7164	SRAM	NMOS/CMOS	IDT	8Kx8	4	8×10^{-2}	125	88-in.	Rad Hard Device. No latchup at LET = 120 (June, 1987)
A	IDT7256	SRAM	NMOS/CMOS	IDT	32Kx8	3	0.1	--	88-in	No latchup at LET = 120 @ T = 90°C Rad Hard Device (Sept, 1988)
A	IDT7256	SRAM	NMOS/CMOS	IDT	32Kx8	2.5	0.2	--	88-in	Latchup at LET = 15 with cross section = 7×10^{-5} cm^2 (Dec, 1987)
A	H6116	SRAM	NMOS/CMOS	HIT	2Kx8	4	$>5 \times 10^{-3}$	--	88-in	Latchup at LET >10; cross section = 1.4×10^{-3} cm^2 (June, 1987)
A	MTSC2568	SRAM	CMOS	MIC	32Kx8	<3	0.6	--	88-in.	No latchup data reported (Dec, 1988)
A	CXK58255	SRAM	CMOS	SNY	32Kx8	6	0.1	--	88-in.	Latchup at LET = 45, cross section = 10^{-3} cm^2 (Dec, 1988)
A	EDH8832C	SRAM	NMOS/CMOS	EDI	32Kx8	3	0.5	200	88-in	Latchup at LET = 30; cross section = 2×10^{-3} cm^2 (Dec, 1988)
A	OW62256	SRAM	NMOS/CMOS	OWI	32Kx8	5	0.4	--	88-in	No latchup at LET = 120 (Dec, 1987)
A	XCDM62256	SRAM	NMOS/CMOS	RCA	32Kx8	3	0.4	--	88-in.	Latch u at LET = 38; cross section = 10^{-3} cm^2 (Dec, 1987)
A	CY7C150	SRAM	CMOS	CYP	1Kx4	--	--	--	88-in.	No soft upset data. Latchup at LET <30; cross section = 10^{-5} cm^2 (June, 1988)
A	SSM7188	SRAM	BICMOS	SST	16Kx4	--	--	--	88-in.	No soft upset data. No latchup at LET = 60 (June, 1988)
J	MA6116	SRAM	CMOS/SOS	MED	2Kx8	>120	--	--	88-in.	No latchup; no SEU. G. Brucker (RCA) believes that this part has a harder technology than that tested by ESA & Aerospace. (April, 198
A	MA6116	SRAM	CMOS/SOS	MED	2Kx8	43	10^{-3} at high LET	--	88-in.	No latchup at LET = 90 (Mar, 1988)
ESA	MA6116	SRAM	CMOS/SOS	MED	2Kx8	32	--	8	88-in.	No latchup. 3-micron technology (Nov, 1988)
ESA	MA9187	SRAM	CMOS/SOS	MED	64Kx1	60	--	≥2	88-in.	No latchup. 1.5-micron technology (Sept, 1988)

Table 1. SEU Data (MOS & CMOS Devices) 1987 & 1988 (Continued)

Test Org*	Device	Function	Technology	M/f	Bits	Effective LET** Threshold (MeV/mg/cm^2)	Device Cross Section (cm^2) ***	Cross Section Per Bit (10^{-8} cm^2)	Facility ****	Remarks (Test Date)
J	HC6167R	SRAM	CMOS (with resistor)	HON	16Kx1	>120	--	--	88-in. BNL	No latchup. High T data available. (Feb & July, 1988)
J	HC6116CHEC	SRAM	CMOS	HON	2Kx8	28	6×10^{-3}	40	88-in	No latchup. High T data available. (Feb & June, 1988)
J	HC6116CHET	SRAM	CMOS	HON	2Kx8	14	6×10^{-3}	40	88-in	No latchup. High T data available. (Feb & June, 1988)
J	V1608	SRAM	CMOS	VTC	2Kx8	15	1.8×10^{-2}	200	BNL	(Feb, 1987)
J	HM6504	SRAM	CMOS	HAR	4Kx1	5	5×10^{-3}	125	88-in	Device also has latchup threshold = 13 (Oct, 1987)
J	HS6504RH	SRAM	CMOS/epi rad-hard	HAR	4Kx1	36	1.2×10^{-3}	30	88-in	Stated s is near threshold Special test of four epi thicknesses (Jan, 1988)
J	HS6504RRH	SRAM	CMOS/epi (with 200KΩ)	HAR	4Kx1	87	No upset	No Upset	88-in	(May & June, 1987, & Jan, 1988)
J	HM6516	SRAM	CMOS/epi (7 micron)	HAR	2Kx8	10	5×10^{-2}	300	88-in BNL	Latchup LET >40 (Feb, Apr, May, June, Aug, 1987)
J	HM6516	SRAM	CMOS/epi (12 micron)	HAR	2Kx8	--	--	--	88-in.	Latchup LET >40 (Apr, May, 1987) See Ref 1.
A	HM6516	SRAM	CMOS	HAR	2Kx8	--	--	--	88-in.	Latchup at LET = 30; cross section = 0.02 cm^2 (March, 1988)
J	HM65162	SRAM	CMOS/epi	HAR	2Kx8	<<40 (latchup)	>>3 x 10^{-3} (latchup)	--	88-in.	Very rapid latchup with Kr (April, 1987)
J	HS65T262RRH	SRAM	CMOS/epi (TTL-compatible)	HAR	16Kx1	20 (transients)	4×10^{-6} (transients)	--	88-in.	Transients (30 ns) seen only in "all 1's" mode. (Oct. & Dec, 1987)
J	HS65C262RRH	SRAM	CMOS/epi (CMOS-compatible)	HAR	16Kx1	~40 (transients)	--	--	88-in.	Transients (30 ns) seen only in "all 1's" mode. (July, 1988)
A	HS65C162	SRAM	CMOS/epi (CMOS-compatible)	HAR	2Kx8	10	4×10^{-2}	--	88-in.	No resistors. No latchup at LET = 60 (April, 1988)
'	AM9ZL44	SRAM	NMOS	AMD	4Kx1	1.6	0.41	10^{-4}	Omay, 88-in.	(Aug, 1985)
'	AM2IL47	SRAM	NMOS	AMD	4Kx1	<1.6	0.41	10^{-4}	Omay, 88-in.	(Aug, 1985)
A	AM99C641	SRAM	CMOS	AMD	64Kx1	~1	0.3	500	88-in.	(March, 1987)
A	IMS1601	SRAM	NMOS/CMOS	INM	64Kx1	~2	0.5	800	88-in.	Latchup at LET = 5 with cross section = 4×10^{-4} cm^2 (June, 1987)
A	IMS1600	SRAM	NMOS/CMOS	INM	64Kx1	~3	0.8	--	88-in.	Latchup at LET >30; cross section = 7×10^{-3} cm^2 (June, 1987)
A	PACE422	SRAM	CMOS	PPS	256x4	~1	--	--	88-in.	Latchup at LET = 10; cross section = 2×10^{-3} cm^2 (June, 1987)

Table 1. SEU Data (MOS & CMOS Devices) 1987 & 1988 (Continued)

Test Org*	Device	Function	Technology	Mfr.	Bits	Effective LET** Threshold (MeV/mg/cm^2)	Device Cross Section (cm^2) ***	Cross Section Per Bit (10^{-8} cm^2)	Facility ****	Remarks (Test Date)
J	IS256	DRAM	NMOS	MIC	256K	1	0.6	240	BNL	Mask 1256 (Aug, 1987)
J	HM6616	PROM	CMOS/epi	HAR	2Kx8	<37	10^{-2}	--	88-in.	Latchup LET = 40 (May, 1987)
J	HS6616 (rad hard)	PROM	CMOS/epi	HAR	2Kx8	--	--	--	BNL	Latchup LET>120 at T = 100°C. (June, 1987)
J	HM6617	PROM	CMOS/epi (7 micron epi)	HAR	2Kx8	12	7×10^{-5}	Surmise only peripheral upset	BNL	Latchup LET>120. (Oct & Dec, 1987)
A	MD27664	EPROM	CMOS	INT	8Kx8	--	--	--	88-in.	(2)
J	HS15530	Manchester Encoder	CMOS	HAR	45	25	5×10^{-5} (extrap.)	--	BNL	(May, 1988)
J	LRH10038Q	Gate Array	HCMOS	LSI	16x4 RAM	34±6	--	15	BNL 88-in.	Only 64K RAM tested. (Oct & Dec,1988)
J	CDI6607	Gate Array	CMOS	LED	--	>75	No upset	No Upset	Orsay	(June, 1985)
J	MB5000	Gate Array	HCMOS/epi (10 microns)	MTA	1792	40	--	250 (at LET=120)	88-in.	Configured as 256x7 RAM. At LET = 120 $\sigma = 5 \times 10^{-3}$ cm^2. (Aug, 1987)
J	MB5000	Gate Array	HCMOS/epi (8 microns)	MTA	1792	25	--	250 (at LET=120)	88-in.	See above remarks. (Aug & Oct, 1987) epi)
A	LL7320Q	Gate Array	CMOS/bulk	LSI	--	--	--	--	88-in.	Latchup at LET = 30; cross section = 10^{-7} cm^2 (Dec, 1988)
A/LSI	LRH9320Q	Gate Array	HCMOS	LSI	64	~30	3×10^{-4}	400	BNL	(Sept, 1987) A: No latchup on epi
			(rad hard)		test				88-in.	at LET = 120 (A: Dec, 1988)
A	EP1210	Logic Array	CMOS	ALT	--	--	--	--	88-in.	No latchup at LET = 100 (June 1988)
A	EP1800	Logic Array	CMOS	ALT	--	--	--	--	88-in.	Latchup at LET = 15; cross section = 1.5×10^{-3} cm^2 (June, 1988)
J	MN5253	A/D Converter (12-Bit)	CMOS	MNC	--	<1.6	$\sim 2 \times 10^{-4}$	--	88-in.	Part is bigger than beam. (June & July, 1988)
A	CO422	Clock Controller	CMOS	VTN	--	--	--	--	88-in.	Latchup test only. No latchup at LET = 60 (April, 1988)

(1) Latchup test only, up to 60°C. No latchup observed at LET = 60. (March, 1988)

(2) Latchup test only Latchup threshold = 21. At T = 25°C, latchup cross section = 7×10^{-5} cm^2; At T = 60°C, latchup cross section = 10^{-4} cm^2. (June 1988)

(3) Latchup test only up to LET <100. No latchup (Dec., 1988)

(4) Latchup test only at 20°C. No latchup observed with 308 MeV I at 60° angle for 10^7 ions/cm^2 (August, 1988)

(5) Latchup test only at room T and 60°C. No latchup observed with 308 MeV I at 60° angle for 10^7 ions/cm^2 (August, October, December, 1988)

(6) Latchup test only at T = 60°C. No latchup observed with 275 MeV I at 60° angle for 10^7 ions/cm^2 (Dec., 1988)

Table 2. SEU Data (Bipolar Devices) - 1987 & 1988

Test Org*	Device	Function	Technology	Mfr.	Bits	Effective LET** Threshold ($MeV/mg/cm^2$)	Device Cross Section (cm^2) ***	Cross Section Per Bit (10^{-8} cm^2)	Facility ****	Remarks (Test Date)
I	F9450	8-Bit Microprocessor	I^3L	FSC	--	11	--	--	88-in.	(Aug & Oct, 1987)
I	SBP9989	16-Bit Microprocessor	I^3L (2-micron)	TDX	--	12	--	--	88-in.	(Dec, 1988)
A	54F74	D F/F	FT^2L	TDX	1	6	9×10^{-5}	9000	88-in.	No latchup at LET = 100 (Sept 1988)
A	54F74	D F/F	FT^2L	SCN	1	8	9×10^{-5}	9000	88-in.	No latchup at LET = 100 (Sept 1988)
A	54F109	JK F/F	FT^2L	SCN	1	10	10^{-4}	10,000	88-in.	No latchup at LET = 100 (Dec, 1988)
I	54F373	Latch	FT^2L	FSC	8	25	2×10^{-5}	250	BNL	(Dec, 1986)
A	74S74	D F/F	ST^2L	TDX	1	20	10^{-4}	10,000	88-in.	No latchup at LET = 100 (Dec, 1988)
I	54ALS373	Latch	$ALST^2L$	TDX	8	8	4.5×10^{-4}	5500	BNL	(Dec, 1986)
I	54LS73	J/K F/F	LST^2L	TDX	4	5	--	--	BNL	(Dec, 1988)
I	93L422	RAM	LT^2L	AMD	256x4	<1	4×10^{-2}	4000	88-in. & BNL	(Aug 1986; June, 1987)
I	82S212	RAM	ST^2L	SCN	256x9	1	2×10^{-2}	1000	BNL	Retest with Br. (June, 1987)
I	93422	RAM	T^2L	AMD	256x4	<1	4×10^{-2}	4000	88-in. & BNL	(Aug 1986; June, 1987)
I	93451	PROM (fusible link)	Schottky TTL Tri-State	FSC	1Kx8	<37	10^{-4}	--	88-in. & BNL	(Aug & Dec, 1987; Jan 1988)
I	AM6012	DAC	Bipolar	AMD	--	15	10^{-6}	--	88-in.	(Mar, 1986)
I	AD562	DAC	Bipolar	ADI	--	15	10^{-6}	--	88-in.	(Mar, 1986)
I	AD573	A/D Converter (10-bit)	Bipolar	ADI	--	<1.6	2.5×10^{-4}	--	88-in.	Part bigger than beam (June & July, 1988)
I	TDC1048J6A	A/D Converter (8-bit)	Bipolar	TRW	279	<1.6	3.5×10^{-4}	--	88-in.	Output registers dominate SEU cross section. (Feb & July, 1988)

IV. TRENDS

Some trends in the recent data are offered here. (1) Two 8-bit microprocessors—the Sandia SA3000 and its equivalent, the Harris HS80C85RH—were tested and found to be hard.*** However, 16-bit and 32-bit microprocessors were much softer. (2) The tested microprocessor peripherals were invariably harder than the parent microprocessor. (3) Parts operated at a higher bias were more resistant to soft errors. (4) None of the STM (France) and TI 54HCxxx logic device families could be made to latch up, even when tested at a slightly elevated temperature (60°C). The data here include a retest of the TI 54HC161 and 54HC165, both of which exhibited latchup in previous tests.[2] The previous two parts and most of the present parts are complementary metal-oxide semiconductor (HCMOS) p-well/bulk devices, but some of the earlier data were also for twin-well technology parts. (5) Our intuition that 54HCTxxx devices will behave similarly to 54HCxxx devices is supported by a very limited data set of the former devices. (6) Test data for the 54AC373 and 54ACT373 latches suggest that this technology is susceptible to latchup. (7) Miscellaneous new data were taken for analog switches, bilateral switches, gate arrays, and programmable read-only memories (PROMS). (8) Several analog-to-digital (A/D) converters were tested to try to establish their LET thresholds. Anomalous device-to-device and test-to-test disparities remain to be resolved.**** However, two bipolar digital-to-analog converters (DACs) had a respectably high LET threshold of 15 MeV/mg/cm^2. (9) CMOS RAMs continued to exhibit a wide range of SEU response. The Marconi MA6116 and Honeywell HC6167R l6K RAMs, using CMOS/silicon-oxide semiconductor (SOS) and feedback resistors, respectively, proved to be very hard. (10) NMOS technology, whether as high density dynamic random access memory (DRAM) or 4K RAMs, had a very low LET threshold. (11) Many new tests were made at higher temperatures—not usually indicated in the tables. When this was done, the parts tested at higher temperatures were always more susceptible to soft errors or latchup.

*** In this context, the term "hard" refers to a part that does not upset with 150 to 350 MeV Kr at normal incidence.

**** Inconsistencies in repeat test data for the ADCs are seen. JPL believes that special test techniques may be required to understand SEUs' effects on ADCs.

V. CONCLUSIONS

The new data presented here can be combined with data given in References 1 and 2 to provide certain generalizations useful for protecting flight electronics from SEP. Hard technologies and unacceptably soft technologies can be flagged. In some instances, specific tested parts can be taken as candidates for key microprocessors or memories. As always with radiation test data, specific test data for qualified flight parts are recommended for critical applications. Calculations of accurate SEP rates will require the assistance of a computer code, a well-defined environment (in terms of flux vs LET), and a complete device characterization (cross section vs LET at the appropriate temperature.)

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APPENDIX
MANUFACTURER ABBREVIATIONS

ADI	Analog Devices, Inc.
ALT	Alpha Industries, Semiconductor Division
AMD	Advanced Microdevices Corporation
CYP	Cypress Corporation
EDI	EDI Corporation
FSC	Fairchild Corporation, Semiconductor Division
HAR	Harris Corporation, Harris Semiconductor Division
HIT	Hitachi Ltd.
HON	Honeywell, Inc.
IDT	Integrated Devices Technology, Inc.
INM	INMOS Corporation
INT	Intel Corporation
LED	Lockheed Corporation
LSI	LSI Logic Corporation
MED	Marconi Electronic Devices
MIC	Micron Technologies
MMI	Monolithic Memories, Inc.
MNC	Micro Networks
MTA	Mattra Harris Semiconductor
NSC	National Semiconductor Corporation
OWI	Omni-Wave, Inc.
PFS	Performance Semiconductor Corporation
SGN	Signetics Corporation
SIL	Siliconix, Inc.
SNL	Sandia National Laboratories
SNY	Sony Corporation
SRT	Saratoga Semiconductor, Inc.

STM	STM (France)
STX	Supertex, Inc.
TIX	Texas Instruments, Inc.
TRW	TRW, Inc.
VTC	VTC, Inc.
VTN	Vectron Corporation
ZIL	Zilog

LABORATORY OPERATIONS

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Chemistry and Physics Laboratory: Atmospheric chemical reactions, atmospheric optics, light scattering, state-specific chemical reactions and radiative signatures of missile plumes, sensor out-of-field-of-view rejection, applied laser spectroscopy, laser chemistry, laser optoelectronics, solar cell physics, battery electrochemistry, space vacuum and radiation effects on materials, lubrication and surface phenomena, thermionic emission, photosensitive materials and detectors, atomic frequency standards, and environmental chemistry.

Electronics Research Laboratory: Microelectronics, solid-state device physics, compound semiconductors, radiation hardening; electro-optics, quantum electronics, solid-state lasers, optical propagation and communications; microwave semiconductor devices, microwave/millimeter wave measurements, diagnostics and radiometry, microwave/millimeter wave thermionic devices; atomic time and frequency standards; antennas, rf systems, electromagnetic propagation phenomena, space communication systems.

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